Approved	Design
Tsumagari	Yazawa

KIOXIA microSDHC Card Specification

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Application

This document describes the specifications of the KIOXIA Standard microSDHC Card. To commence the design of the host system for microSDHC Card, please refer the “9.Host Interface design notes”. The descriptions of microSD in this document may be read as microSDHC fitly.

1. Production Code

KIOXIA Standard microSDHC Card:

	Capacity	Model Name
microSDHC		
	16GB	SD-C16G3K1A (AHHYA)

Fig 1: KIOXIA microSDHC Card Design

2. Product Overview

The microSD Card is a Memory Card of Small and Thin with Flash Memory.

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3. SD Card Features

Table1: SD card Features

Label Design, Contents, Media Format		
Design	KIOXIA Standard (Fig .1)	
Contents	None (OEM Design Available)	ID Programmed (KIOXIA Specific)
Security Functions	SD Security Specification Ver.4.00 Compliant (Non-CPRM) *CPRM: Contents Protection for Recording Media Specification	
Logical Format	SD File System Specification Ver.3.00 Compliant (DOS-FAT Based formatted)	
Physical , Electrical		
Electrical	Operating Voltage: 2.7V to 3.6 V (Memory Operation) Interfaces: SD Card Interface, (SD : 4 or 1bit) SPI Mode Compatible SD Physical Layer Specification Ver.6.10 Compliant	
Physical	L: 15, W: 11, T: 1.0 (mm), Weight: 0.3g (typ.) microSD Card Addendum Ver.4.20 Compliant (Detailed Dimensions attached : sheet . 1)	
Durability	SD Physical Layer Specification Ver.6.10 Compliant microSD Card Addendum Ver.4.20 Compliant	
RoHS	The product(s) is/are compatible with RoHS regulations (EU directive 2011 / 65 / EU) as indicated, if any, on the packaging label ("[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS[[Chemical symbol(s) of controlled substance(s)]]", "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV"),	
Packaging	Appendix5-1,Appendix5-2	

3.1. MOLD

1) Mold
Material : Epoxy Resin+Silicon Dioxide
Flameproof Grade : V-0(UL94)
Heatproof Temperature : approx.400 degrees

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4. Compatibility

Compliant Specifications

- SD Memory Card Specifications
  - Compliant with PHYSICAL LAYER SPECIFICATION Ver.6.10. (Part1)
  - Compliant with FILE SYSTEM SPECIFICATION Ver.3.00. (Part2)
  - Compliant with SECURITY SPECIFICATION Ver.4.00. (Part3)
  - microSD Card Addendum Ver.4.20

Supplementary Explanation are described in “8.Others: Limited Conditions, SD Specification Compliance” in this document.

5. Physical Characteristics

5.1. Temperature

1) Operation Conditions
Temperature Range: Ta = -25 to +85 degrees centigrade

2) Storage Conditions
Temperature Range: Tstg = -40 to +85 degrees centigrade

5.2. Moisture (Reliability)

1) Operation Conditions
Temperature 25 degrees centigrade / 95% rel. humidity

2) Storage Conditions
Temperature 40 degrees centigrade / 93% rel. humidity / 500h

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5.3. Physical Characteristics

1) Hot Insertion or Removal

KIOXIA microSD Card can remove or insert without power off the host system described in the 6.1 of the PHYSICAL LAYER SPECIFICATION.

The connector to realize the Hot Insertion or Removal is defined in the 6.2 of the PHYSICAL LAYER SPECIFICATION.

2) Mechanical Write Protect Switch

microSD memory Card has no mechanical write protect switch.

6. Electrical Interface outlines

6.1. microSD Card Pins

Table 2 describes the pin assignment of the microSD card.
Fig.3 describes the pin assignment of the microSD card.

Please refer the detail descriptions by SD Card Physical Layer Specification.

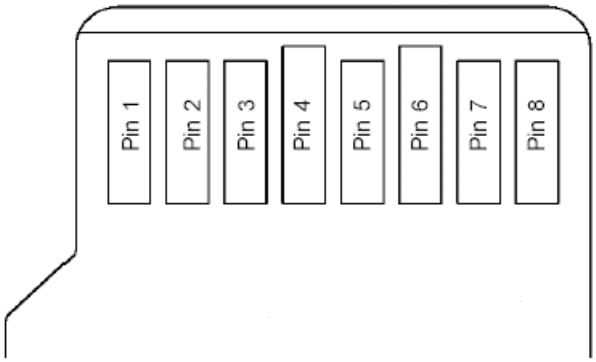

Fig 3: microSD Card Pin assignment (Back view of the Card)

Table 2: microSD card pin assignment

Pins	SD Mode			SPI Mode		
	Name	IO type [1]	Description	Name	IO Type	Description
1	DAT2	I/O /PP	Data Line[Bit2]	RSV		
2	CD/ DAT3	I/O/PP	Card Detect / Data Line[Bit3]	CS	I	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{dd}	S	Supply Voltage	V_{dd}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O /PP	Data Line[Bit0]	DO	O/PP	Data Out
8	DAT1	I/O /PP	Data Line[Bit1]	RSV	-	Reserved (*)

1) S: Power Supply, I: Input, O: Output, I/O: Bi-directionally, 'PP' - IO using push-pull drivers

(*) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.

Do not use NC pins.

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6.2 microSD Card Bus Topology

The microSD Memory Card supports two alternative communication protocols: SD and SPI Bus Mode.

Host System can choose either one of modes. Same Data of the microSD Card can read and write by both modes.

SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel. The disadvantage of this mode is loss of performance, relatively to the SD mode.

6.2.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal.
After power up by default, the microSD card will use only DAT0. After initialization, host can change the bus width.

Multiplied microSD cards connections are available to the host. Common V_{dd}, V_{ss} and CLK signal connections are available in the multiple connection. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host.
This feature allows easy tradeoff between hardware cost and system performance. Communication over the microSD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:
Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to a addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:
Responses are transferred serially on the CMD line.
A response is a token to answer to a previous received command. Responses are sent from a addressed single card or from all connected cards.

Data:
Data can be transfer from the card to the host or vice versa.
Data is transferred via the data lines.

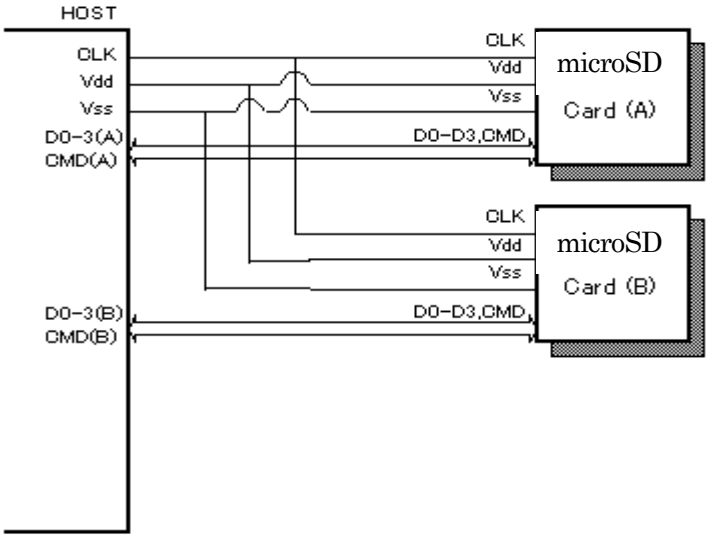

Fig 4: microSD Card (SD Mode) connection Diagram

CLK	: Host card Clock signal
CMD	: Bi-directional Command/ Response Signal
DAT0 - DAT3	: 4 Bi-directional data signal
V_{dd}	: Power supply
V_{ss}	: GND

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Table 3: SD Mode Command Set
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented.
CMD6	SWITCH_FUNC	+	
CMD7	SELECT/DESELECT_CARD	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD11	VOLTAGE_SWITCH	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD19	SEND_TUNING_PATTERN	+	
CMD20	SPEED_CLASS_CONTROL	+	For SDHC/SDXC
CMD23	SET_BLOCK_COUNT	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	-	
ACMD25	SECURE_WRITE_MULTI_BLOCK	-	
ACMD26	SECURE_WRITE_MKB	-	
ACMD38	SECURE_ERASE	-	
ACMD43	GET_MKB	-	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	-	
ACMD46	SET_CER_RN2	-	
ACMD47	SET_CER_RES2	-	
ACMD48	SET_CER_RES1	-	
ACMD49	CHANGE_SECURE_AREA	-	

- CMD28, 29 and CMD30 are Optional Commands.
- CMD4 is not implemented because DSR register (Optional Register) is not implemented.
- CMD56 is for vender specific command. Which is not defined in the standard card.

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6.2.2 SPI Bus mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out).

The SPI compatible mode allows the MMC Host systems to use SD card with little change.
The SPI bus mode protocol is byte transfers.

All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.

The advantage of the SPI mode is reducing the host design in effort.

Especially, MMC host can be modified with little change.

The disadvantage of the SPI mode is the loss of performance versus SD mode.

Caution: Please use SD Card Specification. DO NOT use MMC Specification.

For example, initialization is achieved by ACMD41, and be careful to Register. Register definition is different, especially CSD Register.

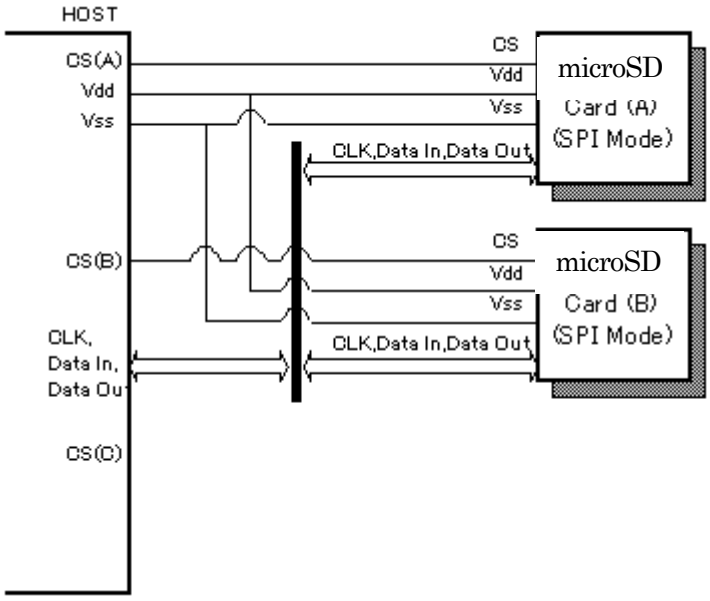

Fig 5: microSD card (SPI mode) connection diagram

CS	:	Card Select Signal
CLK	:	Host card Clock signal
Data in	:	Host to card data line
Data out	:	card to host data line
V_{dd}	:	Power supply
V_{ss}	:	GND

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Table 4: SPI Mode Command set
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (SEE Fig.6 -1and 9.4)
CMD6	SWITCH_FUNC	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	-	
ACMD25	SECURE_WRITE_MULTI_BLOCK	-	
ACMD26	SECURE_WRITE_MKB	-	
ACMD38	SECURE_ERASE	-	
ACMD43	GET_MKB	-	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	-	
ACMD46	SET_CER_RN2	-	
ACMD47	SET_CER_RES2	-	
ACMD48	SET_CER_RES1	-	
ACMD49	CHANGE_SECURE_AREA	-	

- CMD28, 29 and CMD30 are Optional Commends.
- CMD56 is for vender specific command. Which is not defined in the standard card.

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6.3. microSD Card Initialize

Fig.6-1 shows initialization flow chart for UHS-I hosts and Fig.6-2 shows sequence of commands to perform signal voltage switch. Red and yellow boxes are new procedure to initialize UHS-I card.

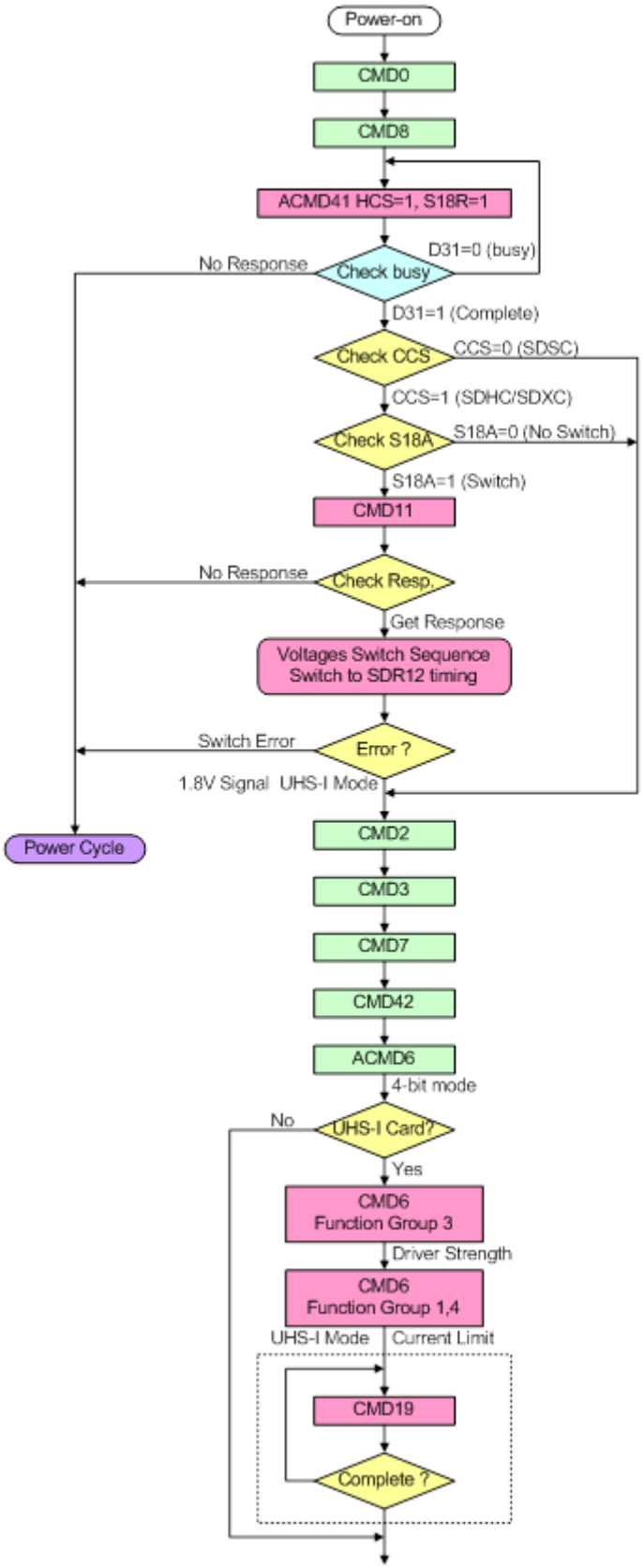

Fig 6-1: UHS-I Host Initialization Flow Chart

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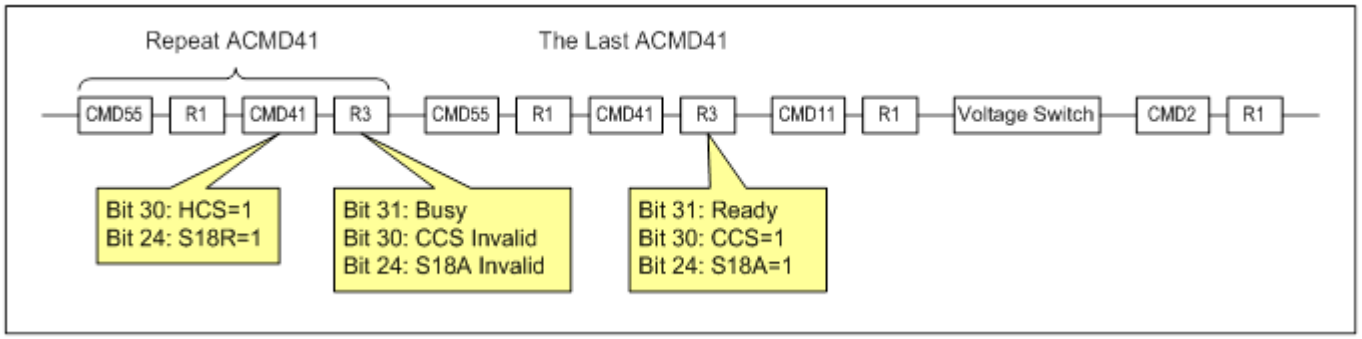

Fig 6-2: ACMD41 Timing Followed by Signal Voltage Switch Sequence

1) POWER ON：Supply Voltage for initialization.

Host System applies the Operating Voltage to the card.

Apply more than 74 cycles of Dummy-clock to the SD card.

2) Select operation mode (SD mode or SPI mode)

In case of SPI mode operation, host should drive CD/DAT3 (SD #1, microSD #2) of SD Card I/F to “Low” level. Then, issue CMD0.In case of SD mode operation, host should drive or detect CD/DAT3 (SD #1, microSD #2) of SD Card I/F (Pull up register of CD/DAT3 is pull up to “High” normally).

Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3) Send Interface condition command (CMD8).

When the card is in Idle state, the host shall issue CMD8 before ACMD41.

In the argument, 'voltage supplied' is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern.

The card that accepted the supplied voltage returns R7 response.

In the response, the card echoes back both the voltage range and check pattern set in the argument.

If the card does not support the host supply voltage, it shall not return response and stays in Idle state.

4) Send initialization command (ACMD41).

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready.

The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument.

If Bit 31 indicates ready, host needs to check CCS and S18A.

The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level.

Table 4-2: S18R and S18A Combinations

Current Signaling Level	18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

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5) Send voltage switch command (CMD11).

S18A=1 means that voltage switch is allowed and host issues CMD11 to invoke voltage switch sequence.
By receiving CMD11, the card returns R1 response and start voltage switch sequence.
No response of CMD11 means that S18A was 0 and therefore host should not have sent CMD11.
Completion of voltage switch sequence is checked by high level of DAT[3:0].
Any bit of DAT[3:0] can be checked depends on ability of the host.
The card enters UHS-I mode and card input and output timings are changed (SDR12 in default) when the voltage switch sequence is completed successfully.

6) Send ALL_SEND_CID command (CMD2) and get the Card ID (CID).

7) Send SEND_RELATIVE_ADDR (CMD3) and get the RCA.

RCA value is randomly changed by access, not equal zero.

8) Send SELECT / DESELECT_CARD command (CMD7) and move to the transfer state.

When entering tran state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7).
If the CARD_IS_LOCKED status is set to 1 in the response of CMD7, CMD42 is required before ACMD6 to unlock the card. (If the card is locked, CMD42 is required to unlock the card.)
If the card is unlocked, CMD42 can be skipped.

9) Send SET_BUS_WIDTH command (ACMD6).

UHS-I supports only 4-bit mode. Host shall select 4-bit mode by ACMD6.
If the card is locked, host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change 4-bit bus mode. Operating in 1-bit mode is not assured.

10) Set driver strength.

CMD6 mode 0 is used to query which functions the card supports, and to identify the maximum current consumption of the card under the selected functions.
In case of UHS-I card, appropriate driver strength (default is Type-B buffer) is selected by CMD6 Function Group 3.

11) Set UHS-I mode current limit.

UHS-I modes (Bus Speed Mode) is selected by CMD6 Function Group 1.
Current Limit is selected by CMD6 Function Group 4.

Note:
Function Group 4 is defined as Current Limit switch for SDR104, SDR50, DDR50.
The Current Limit does not act on the card in SDR12 and SDR25.
The default value of the Current Limit is 200mA (minimum setting).
Then after selecting one of SDR104, SDR50 and DDR50 mode by Function Group 1, host needs to change the Current Limit to enable the card to operate in higher performance.
This value is determined by a host power supply capability to the card, heat release method taken by a host and the maximum current of a connector.

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12) Tuning of sampling point

CMD19 sends a tuning block to the host to determine sampling point.

In SDR104, SDR50 and DDR50 modes, if tuning of sampling point is required, CMD19 is repeatedly issued until tuning is completed

Then the Host can access the Data between the SD card as a storage device.

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Application Notes:

1. The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

2. Once signal voltage is switched to 1.8V, the card continues 1.8V signaling regardless of CMD0. Power cycle resets the signal voltage to 3.3V. After switching 1.8V singling, the card cannot be changed to SPI mode.

3. Timing to Switch Signal Voltage
   To change signaling level at the same time between host and card, signal voltage switch sequence is invoked by CMD11 as shown in Fig.8. CMD11 is issued only when S18A=1 in the response of ACMD41.

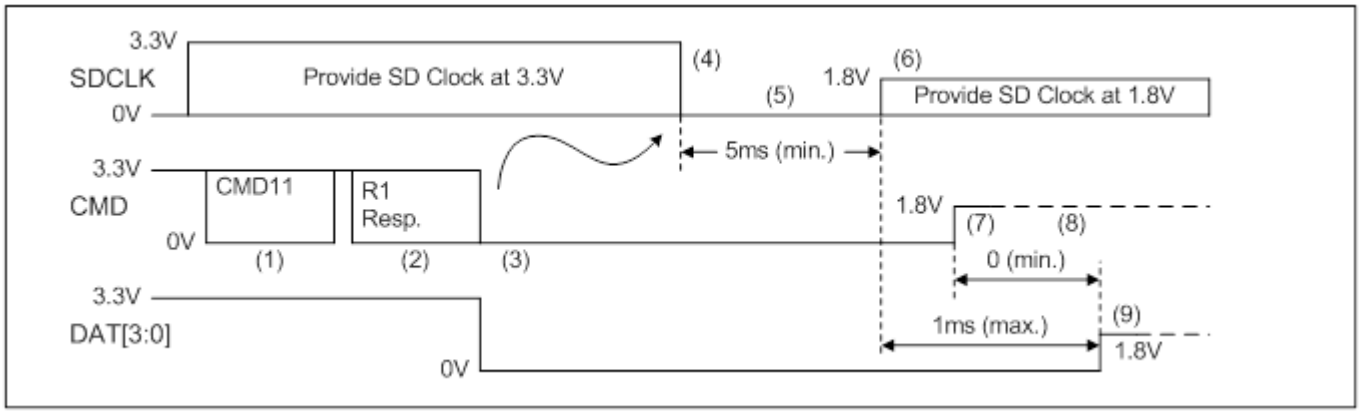

Fig 6-3: Signal Voltage Switch Sequence

(1) Host issues CMD11 to start voltage switch sequence.
(2) The card returns R1 response.
(3) The card drives CMD and DAT[3:0] to low immediately after the response.
(4) The host stops supplying SDCLK. The card shall start switching voltage after host stops SDCLK.
The time to stop SDCLK is not specified. The host can detect whether the sequence starts by checking signal level of either one of CMD, DAT[3:0]. Which signal should be checked depends on ability of the host. If low level is not detected, the host should abort the sequence and execute power cycle.
(5) 1.8V output of voltage regulator in card shall be stable within 5ms. Host keeps SDCLK low at least 5ms.
This means that 5ms is the maximum for the card and the minimum for the host.
(6) After 5ms from (4) and host voltage regulator is stable, the host starts providing SDCLK at 1.8V.
The card can check whether SDCLK voltage is 1.8V.
(7) By detecting SDCLK, the card drives CMD to high at 1.8V at least one clock and then stop driving (tri-state).
CMD is triggered by rising edge of SDCLK (SDR timing).
(8) The card can check whether host drives CMD to 1.8V through the host pull-up resister.

If switching to 1.8V signaling is completed successfully, the card drives DAT[3:0] to high at 1.8V at least one clock and then stop driving (tri-state). DAT[3:0] is triggered by rising edge of SDCLK (SDR timing). DAT[3:0] shall be high within 1ms from start of providing SDCLK. Host check whether DAT[3:0] is high after 1ms from supplying SDCLK. This means that 1ms is the maximum for the card and the minimum for the host.

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6.4. microSD card Electrical Characteristics

(SD Bus Mode)

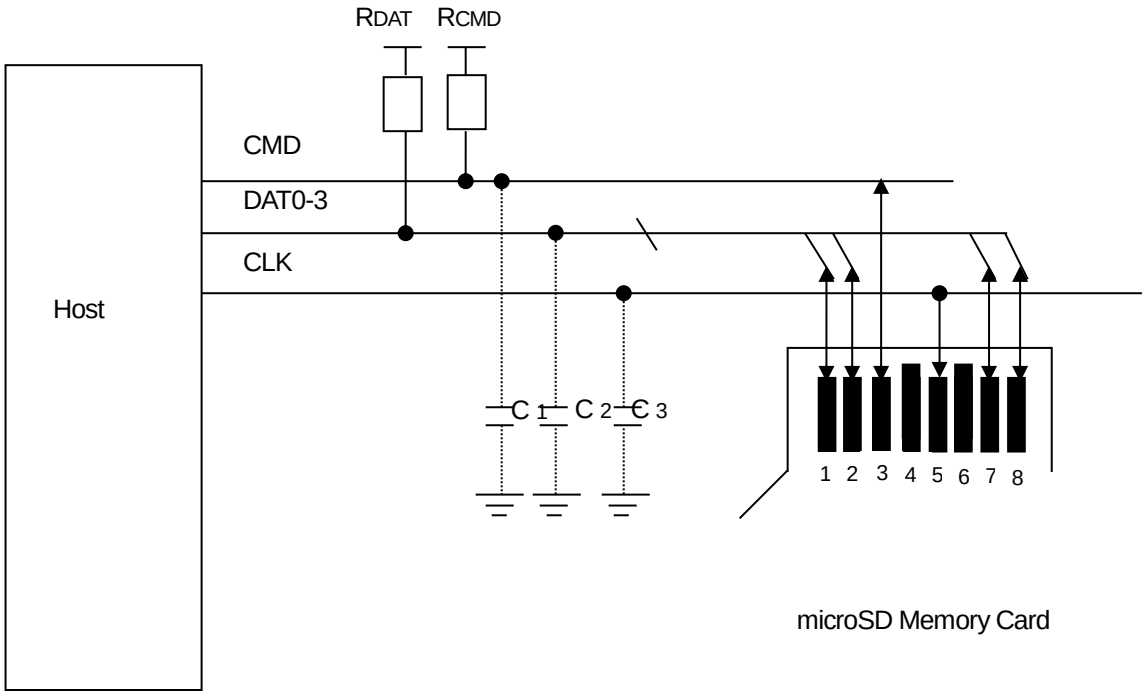

Fig 7: microSD card (SD Bus Mode) Connection diagram

6.4.1 Absolute Maximum Conditions

Table 5: Absolute Maximum Conditions

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 3.9	V
Input Voltage	V_{IN}	-0.3 to 3.9	V

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6.4.2 DC Characteristics

Table 7-1: DC Characteristics (Threshold level for High Voltage Range)

Item		Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Supply Voltage			-	2.7	-	3.6	V	
Input Voltage	High Level	V_{IH}	-	VDDx0.625	-	VDD+0.3	V	
	Low Level	V_{IL}	-	VSS-0.3	-	VDDx0.25	V	
Output Voltage	High Level	V_{OH}	VDD Min IOH = -2mA	VDDx0.75	-	-	V	
	Low Level	V_{OL}	VDD Min IOL = -2mA	-	-	VDDx0.125	V	
Power up Time			-	-	-	250	ms	From 0V to VDD min

*) Peak Current: RMS value over a 10 μs period

Table 7-2: Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	μA	
All Outputs					
Output Leakage Current		-10	10	μA	

Table 7-3: DC Characteristics (Threshold level for 1.8V signaling)

Item		Symbol	MIN.	MAX.	Unit	Condition
Supply Voltage		V_{DD}	2.7	3.6	V	
Regulator Voltage		V_{DDIO}	1.7	1.95	V	Generated by VDD
Input Voltage	High Level	V_{IH}	1.27	2.00	V	
	Low Level	V_{IL}	Vss-0.3	0.58	V	
Output Voltage	High Level	V_{OH}	1.4	-	V	IOH=2mA
	Low Level	V_{OL}	-	0.45	V	IOL=2mA

Table 7-4: Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	μA	DAT3 pull-up is disconnected.

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Table 7-5: Power Consumption

Item	Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Standby Current	I_{CCS}	3.0V Clock Stop	-	-	1350	μA	@25 deg C
Operation Current (peak)	I_{CCOP1} *1)	Current Limit=400mA V_{DD} = 3.6V	-	-	300	mA	@25 deg C
		Current Limit=200mA V_{DD} = 3.6V	-	-	300		
		(HS or DS), V_{DD} = 3.6V			300		
Operation Current (average)	I_{CCOP2} *2)	Current Limit=400mA V_{DD} = 3.6V			250	mA	@25 deg C
		Current Limit=200mA V_{DD} = 3.6V			200		
		SDR25 or HS V_{DD} = 3.6V			200		
		SDR12or DS, V_{DD} = 3.6V			100		

*1) Peak Current: RMS value over a 10 μs period
*2) Average Current: value over 1 sec period.

Table 7-6: Signal Capacitance

Total bus capacitance = CHOST + CBUS + N□ CCARD

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	R_{CMD} R_{DAT}	10	100	k Ohm	
Total bus capacitance for each signal line	C_L	-	40	pF	1 card CHOST+CBUS shall not exceed 30 pF (Note*1)
Card Capacitance for each signal pin	C_{CARD}	-	10	pF	
Maximum signal line inductance			16	nH	
Pull up Resistance inside card(pin1)	R_{DAT3}	10	90	k Ohm	May be used for card detection
Capacity Connected to Power Line	CC		5	μF	To prevent inrush current

Note: WP pull-up (R_{wp}) Value is depend on the Host Interface drive circuit.

*1:
CHOST: the sum of the host capacitance (= total capacitance of the SD Memory Card bus)
CBUS: the bus capacitance.
Total Bus Capacitance = CHOST + CBUS + NCCARD
(N: Number of connect cards)

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6.4.3 AC Characteristics (Default)

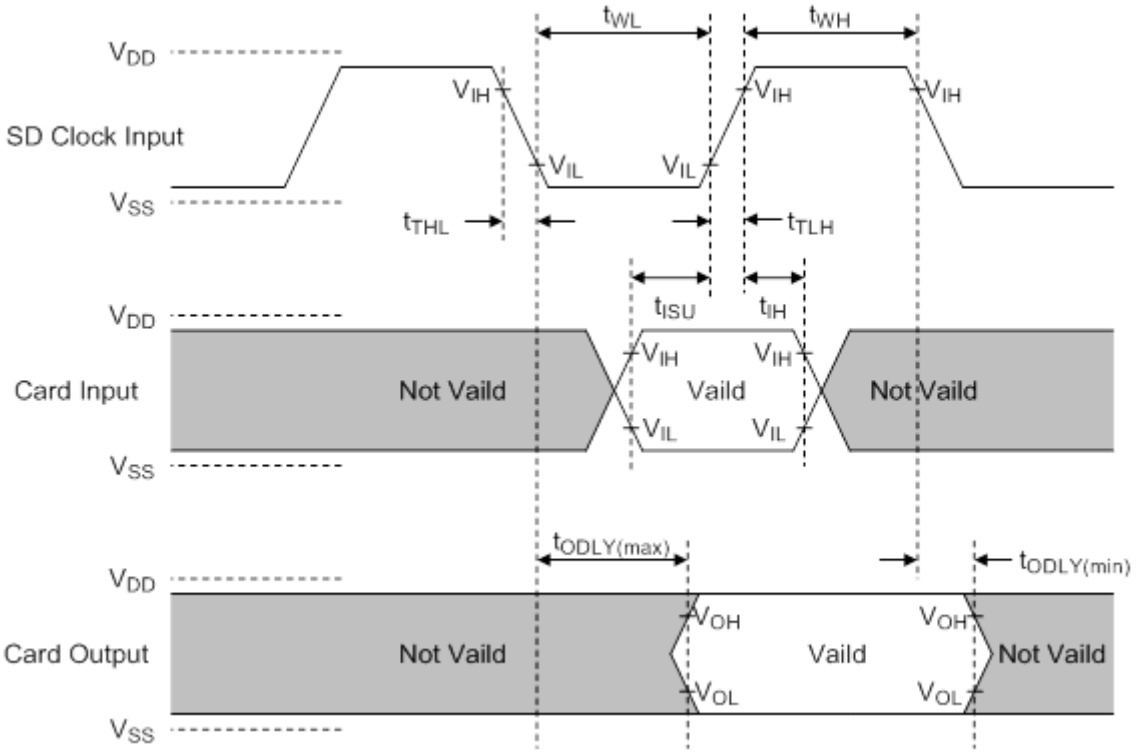

Fig 8-1: AC Timing Diagram (Default)

Table 8-1: AC Characteristics (Default)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In any Sates)	f_{sty}	0	25	MHz	C_{CARD} ≦ 10pF (1Card)
Clock Frequency (Data transfer Mode)	f_{PP}	0	25	MHz	
Clock Frequency (Card identification Mode)	f_{OD}	0/100 (*1)	400	kHz	
Clock Low Time	t_{WL}	10	—	ns	
Clock High Time	t_{WH}	10	—	ns	
Clock Rise Time	t_{TLH}	—	10	ns	
Clock Fall Time	t_{THL}	—	10	ns	
Input set-up Time	t_{ISU}	5	—	ns	
Input Hold Time	t_{IH}	5	—	ns	
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≦ 40pF (1Card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	

(*1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

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6.4.4 AC Characteristics (High-Speed)

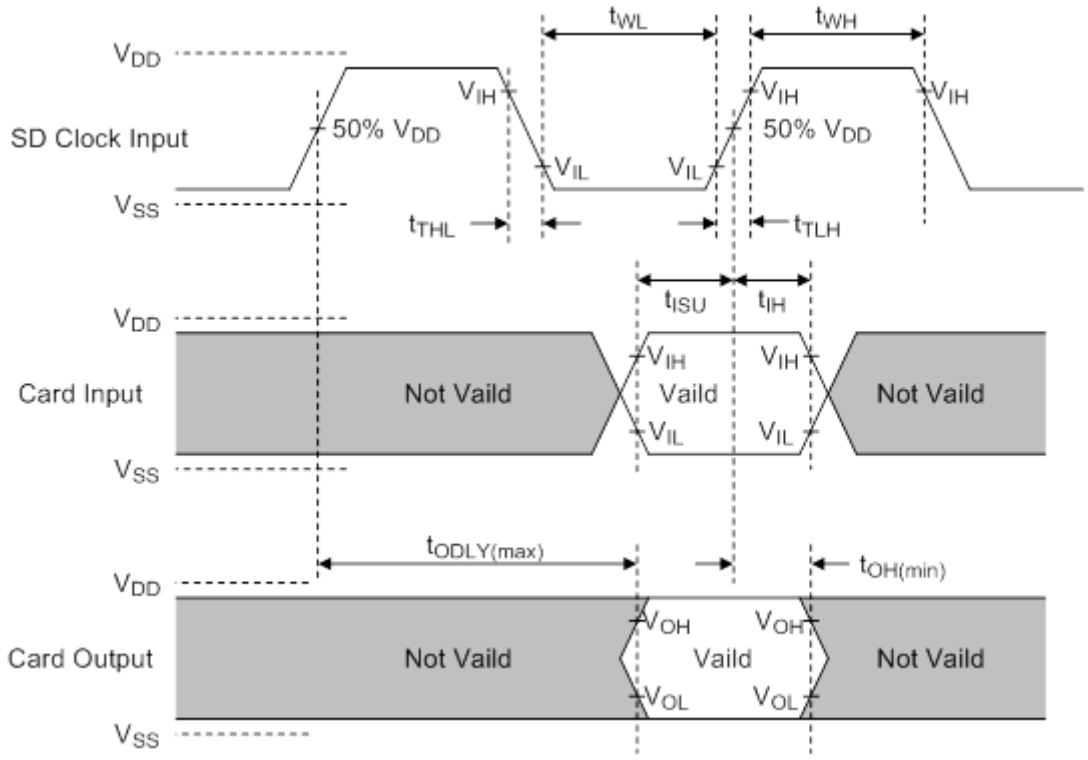

Fig 8-2: AC Timing Diagram (High-Speed)

Table 8-2: AC Characteristics (High-Speed)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (During Data transfer)	f_{PP}	0	50	MHz	Ccard≤10pF (1card)
Clock Low Time	t_{WL}	7	—	ns	Ccard≤10pF (1card)
Clock High Time	t_{WH}	7	—	ns	Ccard≤10pF (1card)
Clock Rise Time	t_{TLH}	—	3	ns	Ccard≤10pF (1card)
Clock Fall Time	t_{THL}	—	3	ns	Ccard≤10pF (1card)
Input Setup Time	t_{ISU}	6	—	ns	Ccard≤10pF (1card)
Input Hold Time	t_{IH}	2	—	ns	Ccard≤10pF (1card)
Output Delay Time	T_{ODLY}	—	14	ns	Ccard≤10pF (1card)
Output Hold Time	T_{OH}	2.5	-	ns	Ccard≤10pF (1card)
Total System capacitance for each line	C_L	-	40	pF	Ccard≤10pF (1card)

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6.4.5 AC Characteristics (SDR12, SDR25, SDR50, SDR104 modes)

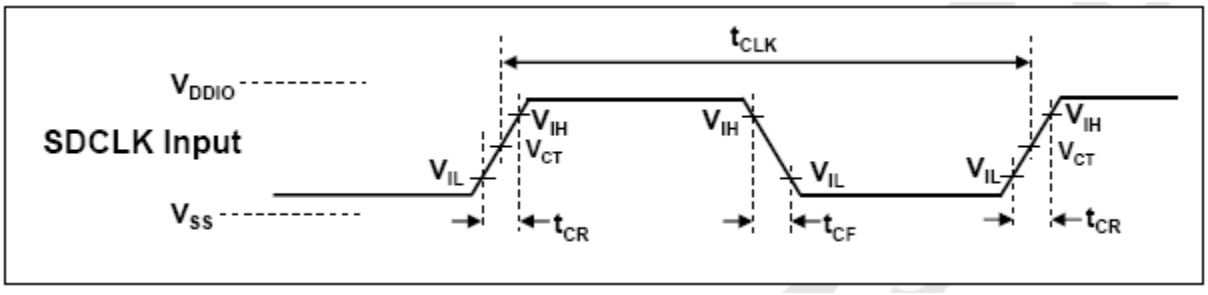

Fig 8-3: AC Timing Diagram (SDR12, SDR25, SDR50, SDR104 modes input)

Table 8-3: AC Characteristics (SDR12, SDR25, SDR50, SDR104 modes input)

Symbol	Min	Max	Unit	Remark
tCLK	4.80	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2x tCLK	ns	tCR, tCF < 0.96ns (max.) at 208MHz, CCARD=10pF tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF The absolute maximum value og tCR, TCF is 10ns regardless of clock frequency.
Clock Duty	30	70	%	-

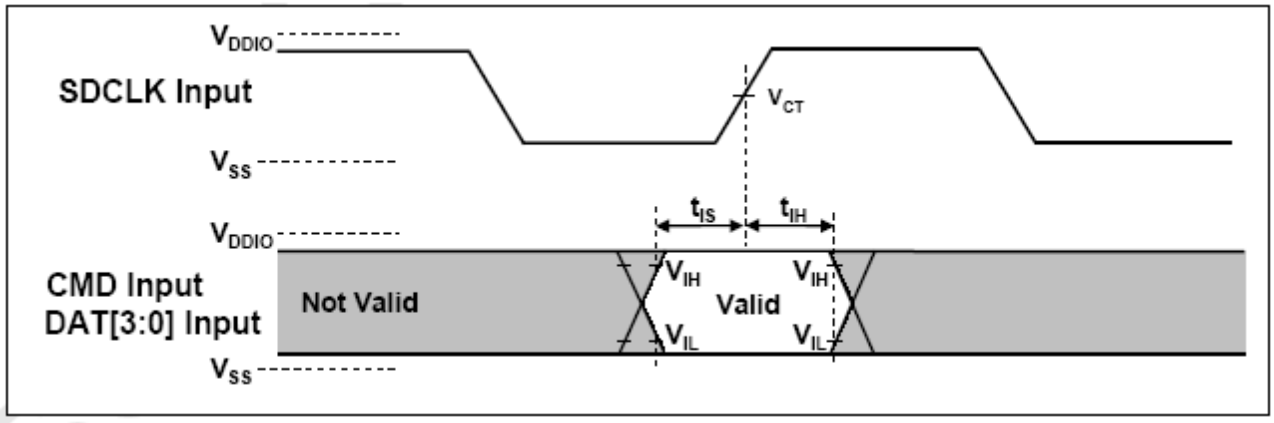

Fig 8-4: AC Timing Diagram (SDR12, SDR25, SDR50, SDR104 input timing)

Table 8-4: AC Characteristics (SDR12, SDR25, SDR50, SDR104 input timing)

Symbol	**Min**	**Max**	**Unit**	**SDR104 Mode**
tIs	1.40	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR12, SDR25, SDR50 Mode**
tIs	3.00	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V

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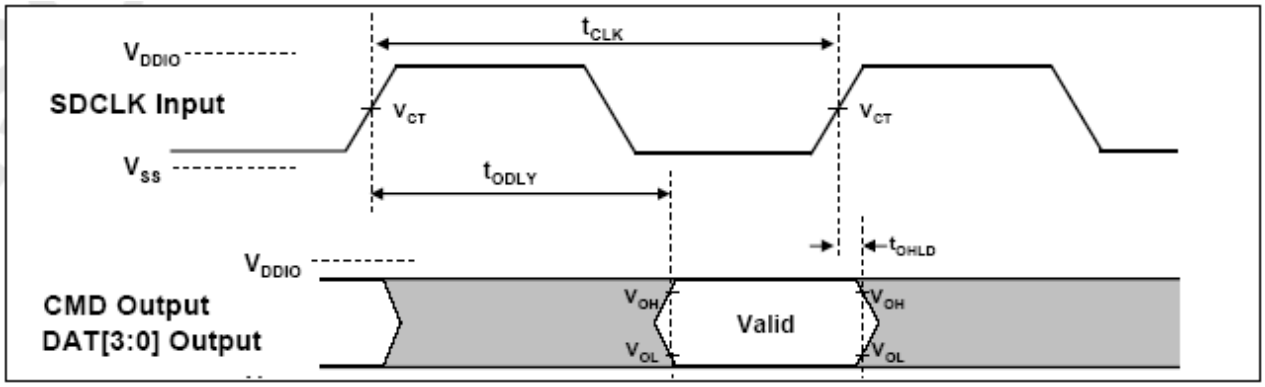

Fig 8-5: Output timing of fixed data window (SDR12, SDR25, SDR50)

Table 8-5: Output timing of fixed data window (SDR12, SDR25, and SDR50)

Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

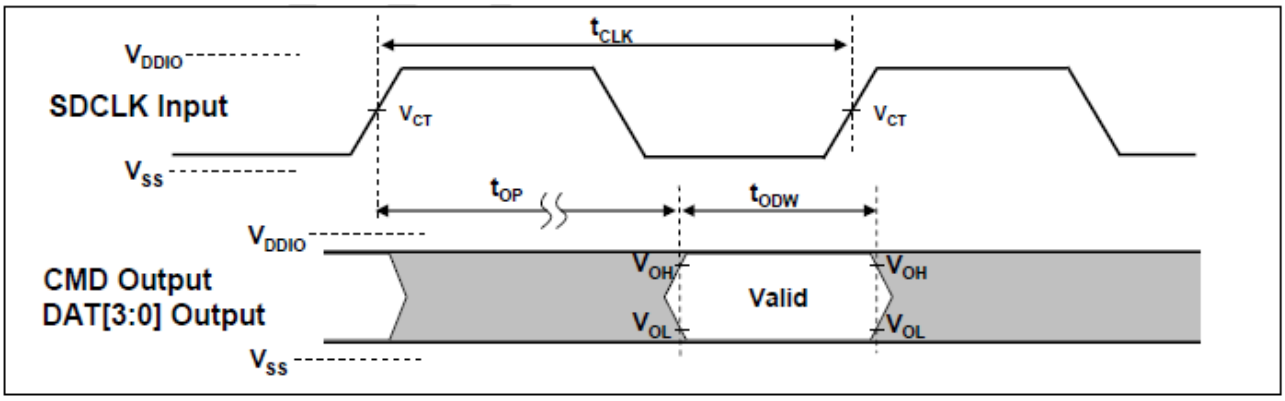

Fig 8-6: Output timing of fixed data window (SDR104)

Table 8-6: Output timing of fixed data window (SDR104)

Symbol	Min	Max	Unit	Remark
tOP	-	2	UI	Card Output Phase
ΔtOP	-350	+1550	ps	Delay variation due to temperature changing after tuning.
tODW	0.60	-	UI	tODW=2.88ns @208MHz

Note: UI (Unit Interval) is one bit normal time, SDCLK normal period.
ΔtOP is the total allowable shift of output valid window (TODW) from last system tuning procedure.

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6.4.6 AC Characteristics (DDR50 mode)

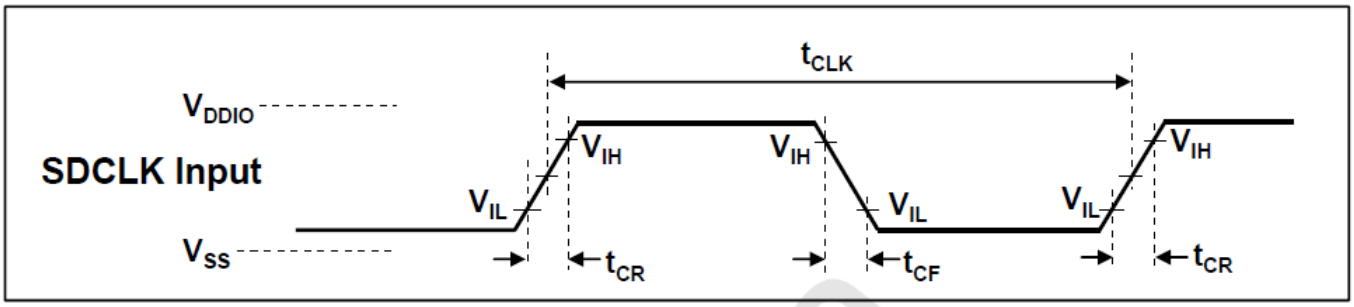

Fig 8-7: Clock signal timing (DDR50 mode)

Table 8-7: Clock signal timing (DDR50 mode)

Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2x tCLK	ns	tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

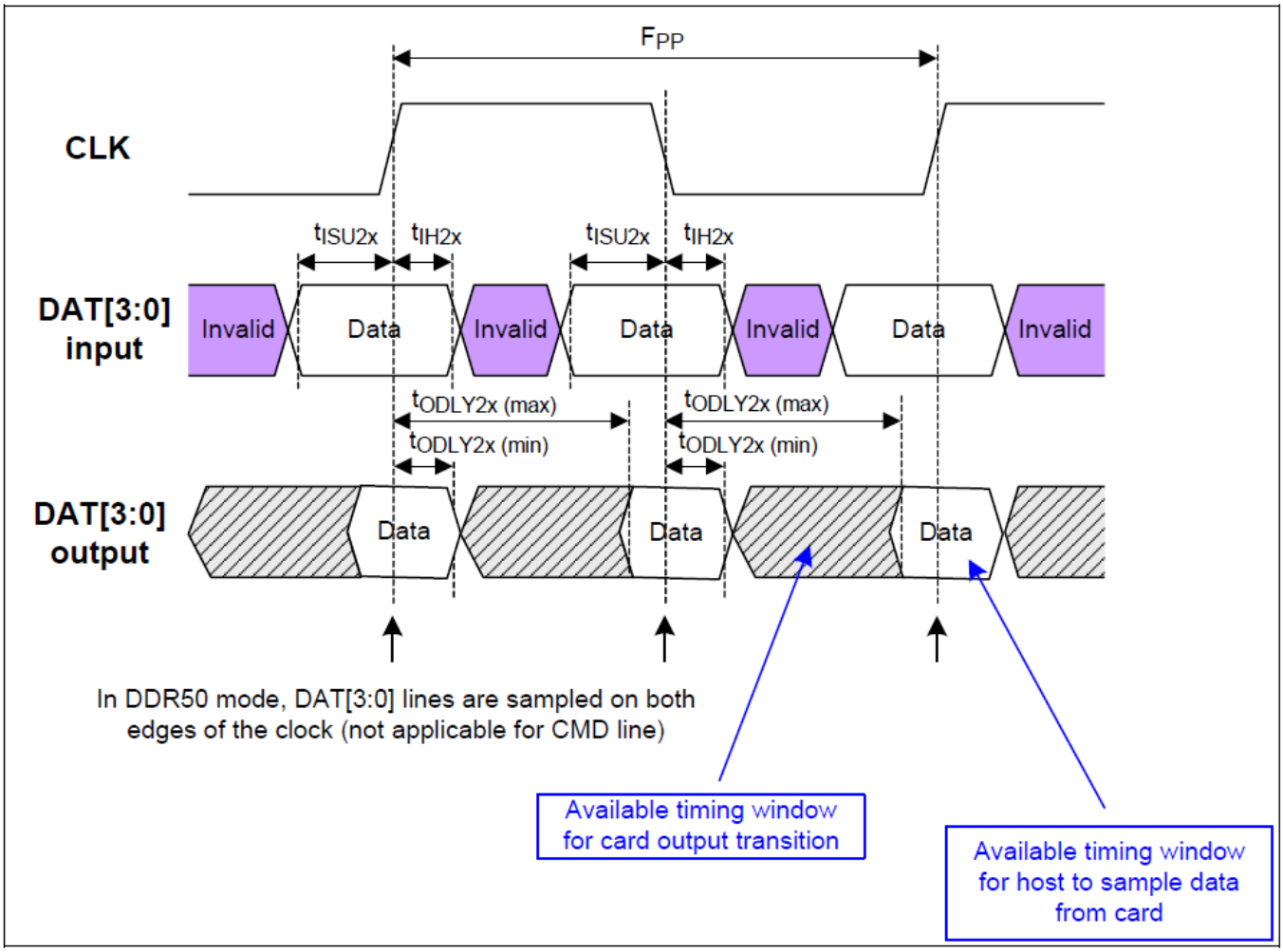

Fig 8-8: Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 mode

CMD signal timings are not shown in Fig8-8. For CMD signal timing refer to Fig8-4 and Fig8-5 and Fig8-6 (Timing Diagram of SDR mode).

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Table 8-8: Bus Timings Parameter Values (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

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7. Card Internal Information

7.1. Security Information

Media ID is KIOXIA Standard Information. MKB (Media Key Block) is not been written.
This card is not CPRM compliant.

7.2. Logical Format

KIOXIA SD card is formatted before shipping compliant to the SD Card FILE SYSTEM SPECIFICATION.
Following parameters may be changed if the host system is not compliant with the SD Card Format Specification.
The logical format parameters are described in the Table 11, 12, 13, 14, 15.
The data of the logical format is described in Appendix 2.

7.2.1. SD card Capacities

Table 11: SD Card capacities

Item	Card Capacities	
	16GB	
	Sector	KB
Whole Capacity	30,507,008	15,253,504
User Data Area Size	30,375,936	15,187,968
Protected Area Size	-	-

7.2.2. SD card System information

Table 12: SD card System information

Item		Card Capacities
		16GB
User Data Area	Data Boundary unit size (KB)	4,096
	Cluster Size(KB)	32
Protected Area	Data Boundary unit size (KB)	-
	Cluster Size(KB)	-

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7.2.3. MBR, Boot Sector parameters

Table 13: Master Boot Record a Partition Table

BP	Data Length	Field Name	Contents
			16GB
0	446	Master Boot Record	All 0x00
446	16	Partition Table(partition1)	Refer Table 14
462	16	Partition Table(partition2)	All 0x00
478	16	Partition Table(partition3)	All 0x00
494	16	Partition Table(partition4)	All 0x00
510	2	Signature Word	0x55(BP510),0xAA(BP511)

Table 14: Partition Table

BP	Data Length	Field Name	Contents
			16GB
0	1	Boot Indicator	0x00
1	1	Starting Head	130
2	2	Starting Sector/Starting Cylinder	3/0
4	1	System ID	0x0C
5	1	Ending Head	254
6	2	Ending Sector/Ending Cylinder	63/1023
8	4	Relative Sector	8192
12	4	Total Sector	30,367,744

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Table 15: Extended FDC Descriptor (FAT32)

BP	Data Length	Field Name	Contents
			16GB
0	3	Jump Command	0xEB(BP0),0x00(BP1),0x90(BP2)
3	8	Creating System Identifier	(Card Specific 8Byte-Data)
11	2	Sector Size	512
13	1	Sectors per Cluster	64
14	2	Reserved Sector Count	778
16	1	Number of FATs	2
17	2	Number of Root-directory Entries	0
19	2	Total Sectors	0
21	1	Medium Identifier	0xF8
22	2	Sectors per FAT	0
24	2	Sectors per Track	63
26	2	Number of Sides	255
28	4	Number of Hidden Sectors	8,192
32	4	Total Sectors	30,367,744
36	4	Sectors per FAT for FAT32	3,707
40	2	Extension Flag	0
42	2	FS Version	0
44	4	Root Cluster	2
48	2	FS Info	1
50	2	Backup Boot Sector	6
52	12	Reserved	All 0x0
64	1	Physical Disk Number	0x80
65	1	Reserved	0x00
66	1	Extended Boot Record Signature	0x29
67	4	Volume ID Number	(Card Specific 4Byte Data)
71	11	Volume Label	“NO NAME “
82	8	File System Type	“FAT32“
90	420	(Reserved for system use)	All 0x00
510	2	Signature Word	0x55(BP510), 0xAA(BP511)

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7.3. SD Card Registers

The SD card has six registers and SD Status information: OCR, CID, CSD, RCA, DSR, SCR and SD Status.
DSR IS NOT SUPPORTED in this card.

There are two types of register groups.

MMC compatible registers: OCR, CID, CSD, RCA, DSR, and SCR
SD card Specific: SD Status

Table 16: SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Conditions (VDU Voltage Profile and Busy Status Information)
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative Card Address
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SD Memory Card's special features
SD Status	512	Status bits and Card features

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7.3.1. OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply.

Table 17: OCR register definition

OCR bit position	VDD voltage window	Initial value
		16GB
31	Card power up status bit (busy)	“0” = busy “1” = ready
30	Card Capacity Status	“0”=SD Memory Card “1”=SDHC or SDXC Memory Card
29-25	Reserved	All ‘0’
24	Switching to 1.8V Accepted(S18A)	1
23	3.6 – 3.5	1
22	3.5 – 3.4	1
21	3.4 – 3.3	1
20	3.3 – 3.2	1
19	3.2 – 3.1	1
18	3.1 – 3.0	1
17	3.0 – 2.9	1
16	2.9 – 2.8	1
15	2.8 – 2.7	1
14	Reserved	0
13	Reserved	0
12	Reserved	0
11	Reserved	0
10	Reserved	0
9	Reserved	0
8	Reserved	0
7	Reserved for Low Voltage Range	0
6	Reserved	0
5	Reserved	0
4	Reserved	0
3-0	reserved	All ‘0’

bit 23-4: Describes the SD Card Voltage
bit 31 indicates the card power up status. Value “1” is set after power up and initialization procedure has been completed.

7.3.2. CID Register

The CID (Card Identification) register is 128-bit width. It contains the card identification information.
The Value of CID Register is vender specific.

Tabel.18: CID Register

Field	Width	CID-slice	Initial Value
			16GB
MID	8	[127:120]	02 h
OID	16	[119:104]	“TM” (544D h)
PNM	40	[103:64]	“SA16G”
PRV	8	[63:56]	(a) Product revision
PSN	32	[55:24]	(b) Product serial number
-	4	[23:20]	All ‘0’
MDT	12	[19:8]	(c) Manufacture date
CRC	7	[7:1]	(d) CRC
-	1	[0:0]	1

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(a), (b), (c): Depends on the SD Card. Controlled by Production Lot.
(d): Depends on the CID Register

7.3.3. CSD Register

CSD is Card-Specific Data register provides information on 128bit width.
Some field of this register can writable by PROGRAM_CSD (CMD27).

Table 19: CSD Register

				Initial Value
Field	Width	Cell Type(1)	CSD slice	**16GB**
CSD_STRUCTURE	2	R	[127:126]	01
-	6	R	[125:120]	Reserved
TAAC	8	R	[119:112]	0_0001_110(1ms)
NSAC	8	R	[111:104]	00000000
TRAN_SPEED	8	R	[103:96]	32h or 5Ah or 0Bh or 2Bh
CCC	12	R	[95:84]	0_1_0_1_1_0_1_1_0_1_0_1
READ_BL_LEN	4	R	[83:80]	1001 (512Bytes)
READ_BL_PARTIAL	1	R	[79:79]	0
WRITE_BLK_MISALIGN	1	R	[78:78]	0
READ_BLK_MISALIGN	1	R	[77:77]	0
DSR_IMP	1	R	[76:76]	0
-	6	R	[75:70]	Reserved
C_SIZE	22	R	[69:48]	73DFh
-	1	R	[47:47]	Reserved
ERASE_BLK_EN	1	R	[46:46]	1
SECTOR_SIZE	7	R	[45:39]	11_1111_1
WP_GRP_SIZE	7	R	[38:32]	000_0000
WP_GRP_ENABLE	1	R	[31:31]	0
-	2	R	[30:29]	00
R2W_FACTOR	3	R	[28:26]	010
WRITE_BL_LEN	4	R	[25:22]	1001
WRITE_BL_PARTIAL	1	R	[21:21]	0
-	5	R	[20:16]	Reserved
FILE_FORMAT_GRP	1	R	[15:15]	0
COPY	1	R/W(1)	[14:14]	0
PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	0
TMP_WRITE_PROTECT	1	R/W	[12:12]	0
FILE_FORMAT	2	R	[11:10]	00
-	2	R	[9:8]	Reserved
CRC	7	R/W	[7:1]	(CRC)
-	1	-	[0:0]	1

Cell Types: R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable
Note: Erase of one data block is not allowed in this card. This information is indicated by “ERASE_BLK_EN”.
Host System should refer this value before one data block size erase.

7.3.4. RCA Register

The writable 16bit relative card address register carries the card address in SD Card mode.

7.3.5. DSR Register

This register is not implemented on this card

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7.3.6. SCR Register

SCR (SD Card Configuration Register) provides information on SD Memory Card's special features.
The size of SCR Register is 64 bit.

Table 20: SCR Register

Field	Width	Cell Type	SCR Slice	Value
				16GB
SCR_STRUCTURE	4	R	[63:60]	0000
SD_SPEC	4	R	[59:56]	0010
DATA_STAT_AFTER_ERASE	1	R	[55:55]	0
SD_SECURITY	3	R	[54:52]	000
SD_BUS_WIDTHS	4	R	[51:48]	0101
SD_SPEC3	1	R	[47]	1
EX_SECURITY	4	R	[46:43]	0000
SD_SPEC4	1	R	[42]	0
SD_SPECX	4	R	[41:38]	0010
reserved	2	R	[37:36]	Reserved
CMD_SUPPORT	4	R	[35:32]	0011
reserved for manufacture usage	32	R	[31:0]	Reserved

(*) R: Read Only

7.3.7. SD Status

Table 21: SD Status

Identifier	Width	Type	SD Status Slice	Value
				16GB
DAT_BUS_WIDTH	2	SR	[511:510]	00 or 10
SECURED_MODE	1	SR	[509]	0
-	13	-	[508:496]	Reserved
SD_CARD_TYPE	16	SR	[495:480]	0x0000
SIZE_OF_PROTECTED_AREA	32	SR	[479:448]	0x00000000
SPEED_CLASS	8	SR	[447:440]	0x04
PERFORMANCE_MOVE	8	SR	[439:432]	0x03
AU_SIZE	4	SR	[431:428]	1001
-	4	-	[427:424]	Reserved
ERASE_SIZE	16	SR	[423:408]	0x0200
ERASE_TIMEOUT	6	SR	[407:402]	0x0C
ERASE_OFFSET	2	SR	[401:400]	0x03
UHS_SPEED_GRADE	4	SR	[399:396]	0x1
UHS_AU_SIZE	4	SR	[395:392]	0x9
VIDEO_SPEED_CLASS	8	SR	[391:384]	0x00
-	6	-	[383:378]	Reserved
VSC_AU_SIZE	10	SR	[377:368]	0x000
SUS_ADDR	22	SR	[367:346]	0x000000
-	6	-	[345:340]	Reserved
APP_RERF_CLASS	4	SR	[339:336]	0x0
PERFORMANCE_ENHANCE	8	SR	[335:328]	0x00
-	14	-	[327:314]	Reserved
DISCARD_SUPPORT	1	SR	[313]	0
FULE_SUPPORT	1	SR	[312]	0
-	312	-	[311:0]	Reserved for manufacturer

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7.4 SD Card Registers Information

The SD card has six registers and SD Status information: CID, CSD, SCR and SD Status.

7.4.1. CID Register

The CID (Card Identification) register is 128-bit width. It contains the card identification information.
The Value of CID Register is vender specific.

- **MID**
  8 bit binary number, Indicates the Manufacture ID allocated by the SDA.
  →02 -h (Indicates KIOXIA) (Unit: -h means Hex-decimal value, here after)

- **OID**
  16 bit binary number, Indicates the Manufacture ID allocated by the SDA.
  →544D -h = "TM" in ASCII String (Indicates KIOXIA)

- **PNM**
  5 ASCII Characters long (40 bit) ,KIOXIA Product Code.
  → KIOXIA Standard SD card indicates as below by capacity.

- **PRV**
  Product Revision of the card.

- **PSN**
  32 bit serial number of unsigned integer.
  → Uniquely assigned integer

- **MDT**
  The manufacturing date composed of two-hexadecimal digits.
  → CID-Slice [11:8] Month Field (Exp. 1h = January)
  CID-Slice [19:12] Year Field (Exp. 0h = 2000)

- **CRC**
  Checksum of CID contents. → CRC 7 Checksum (See Chapter 7. of the SD PHYSICAL SPECIFICATION)

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7.4.2. CSD Register

・CSD_STRUCTURE

Version number of the related CSD structure.

Table 22-1: CSD_STRUCTURE

CSD_STRUCTURE	CSD STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION Version
0	CSD Version 1.0	Standard Capacity
1	CSD Version 2.0	High Capacity and Extended Capacity
2-3	Reserved	

・TAAC

Defines the asynchronous part of the data access time.

Table 22-2: TAAC Access Time Definition

TAAC bit	Code
2:0	Time Unit 0 = 1ns,1 = 10ns,2 = 100ns,3 = 1µs,4 = 10µs,5 = 100µs, 6 = 1ms,7 = 10ms
6:3	Time Value 0 = Reserved,1 = 1.0,2 = 1.2,3 = 1.3,4 = 1.5,5 = 2.0, 6 = 2.5, 7 = 3.0,8 = 3.5,9 = 4.0,A = 4.5,B = 5.0,C = 5.5,D = 6.0, E = 7.0,F = 8.0
7	Reserved

・NSAC

Defines the worst case for the clock dependent factor of the data access time.

Unit is 100 clock cycle.

Total access time equal TAAC plus NSAC, calculation with actual clock frequency.

This is average delay by the first clock output for data block.

・TRAN_SPEED

The following table defines the maximum data transfer rate per one data line.

Table 22-3: Maximum Data Transfer Rate Definition

TRAN_SPEED bit	Code
2:0	Transfer Rate Unit 0 = 100kbit/s,1 = 1Mbit/s,2 = 10Mbit/s,3 = 100Mbit/s, 4-7 = Reserved
6:3	Time Value 0 = Reserved,1 = 1.0,2 = 1.2,3 = 1.3,4 = 1.5,5 = 2.0, 6 = 2.5, 7 = 3.0,8 = 3.5,9 = 4.0,A = 4.5,B = 5.0,C = 5.5,D = 6.0, E = 7.0,F = 8.0
7	Reserved

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・CCC

The Card Class Command Register (CCC) defines which command classes are supported by this card.

Table 22-4: Supported Card Command Classes

CCC bit	Supported Card command Class
0	Class 0
1	Class 1
...	
11	Class 11

・READ_BL_LEN

The Maximum read data block length for reading is computed as $2^{READ\_BL\_LEN}$.
READ_BL_LEN is always equal to WRITE_BL_LEN.

Table 22-5: DATA Block Length

READ_BL_LEN	Block Length
0-8	Reserved
9	2^9 = 512Bytes
・・・	
11	2^{11} = 2048Bytes
12-15	Reserved

・READ_BL_PARTIAL

This field is fixed “0”.

・WRITE_BLK_MISALIGN

Define whether the data block to be written by one command can be spread over more than one physical block of the Flash Memory Device.

Table 22-6: WRITE_BLK_MISALIGN

WRITE_BLK_MISALIGN	Across Block Boundaries Write
0	Not Allowed
1	Allowed

・READ_BLK_MISALIGN

Define whether the data block to be read by one command can be spread over more than one physical block of the Flash Memory Device.

Table 22-7: READ_BLK_MISALIGN

READ_BLK_MISALIGN	Across Block Boundaries Read
0	Not Allowed
1	Allowed

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・DSR_IMP

If set, a driver stage register (DSR) is implemented (supported).

Table 22-8: DSR_IMP

DSR_IMP	DSR Type
0	DSR NOT Implemented
1	DSR Implemented

・C_SIZE

This parameter is used to compute the user's data card capacity (Not include the security area) as below.

Memory Capacity = (C_SIZE + 1) * 512 KB

・ERASE_BLK_EN

(Caution!: This is different from MMC. Please be careful.)

WRITE_BL_LEN defines whether erase of one write block (see WRITE_BL_LEN) is allowed.

Table 22-9: ERASE_BLK_EN

ERASE_BLK_EN	Description
0	Host cannot erase by WRITE_BL_LEN
1	Host can erase by WRITE_BL_LEN

・SECTOR_SIZE

This field is fixed to "11_1111_1". This value does not relate to erase operation. On this cards memory boundary is indicated by AU size and this field should not be used.

・WP_GRP_SIZE

This field is fixed "0x00". The high capacity SD Memory card does not support write protected groups.

・WP_GRP_ENABLE

This field is fixed "0". The high capacity SD Memory card does not support write protected groups.

Table 22-10: WP_GRP_ENABLE

WP_GRP_ENABLE	Description
0	NOT Implemented
1	Implemented

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・R2W_FACTOR

This field is fixed to “0x2”, which indicates 4 multiples. However, host should not use this factor and should use 250ms for write timeout.

Table 22-11: R2W_FACTOR

R2W_FACTOR	Multiples of read Access Time
0	1
1	2(Write half as fast as read)
2	4
3	8
4	16
5	32
6,7	Reserved

・WRITE_BL_LEN

The maximum write block length is calculated as $2^{WRITE\_BL\_LEN}$.

Table 22-12: DATA Block Length

WRITE_BL_LEN	Block Length
0-8	Reserved
9	2^9 = 512Bytes
・・・	
11	2^{11} = 2048Bytes
12-15	Reserved

・WRITE_BL_PARTIAL

This field is fixed to “0”, which indicates partial block is inhibited and only unit of block access is allowed.

Table 22-13: Write Data size

WRITE_BL_PARTIAL	Block Oriented write Data size
0	Only the WRITE_BL_LEN size or 512Bytes are available
1	Partial size (Minimum 1Byte) write available

・FILE_FORMAT_GRP

This field is set to “0”. Host should not use this field.

・COPY

Defines the contents of this card is original (=0) or duplicated (1).
This bit is one time programmable.

Table 22-14: COPY

COPY	Description
0	Original
1	Copy

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・PERM_WRITE_PROTECT

Permanently protects the whole card content against write or erase.
This bit is one time programmable.

Table 22-15: PERM_WRITE_PROTECT

PERM_WRITE_PROTECT	Description
0	Not protected/Writable
1	Permanently Write protected

・TMP_WRITE_PROTECT

Temporarily protects the whole card content against write or erase.

Table 22-16: TMP_WRITE_PROTECT

TMP_WRITE_PROTECT	Description
0	Not protected/Writable
1	Temporarily Write Erase protected

・FILE_FORMAT

This field is set to “0”. Host should not use this field.

Table 22-17: File Format

FILE_FORMAT	Kinds
0	Hard disk-like File system with partition table
1	DOS FAT(floppy-like) with boot sector only (No partition table)
2	Universal File Format
3	Others/Unknown
0,1,2,3	Reserved

・CRC

Calculated CRC for default data is set here.
Host System is responsible to re-calculate this CRC if any CSD contents are changed.

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7.4.3. SCR Register

・SCR_STRUCTURE

Version number of the related structure in the SD Card PHYSICAL LAYER SPECIFICATION.

Table 23-1: SCR_STRUCTURE

SCR_STRUCTURE	SCR STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION
0	SCR Version 1.0	Version 1.01-5.00
1-15	Reserved	

・SD_SPEC, SD_SPEC3, SD_SPEC4, SD_SPECX

Describes the SD PHYSICAL LAYER SPECIFICATION version supported by this card.
Please check the SD Physical Layer Specification for details.

Table 23-2: SD PHYSICAL LAYER SPECIFICATION Version

SD_SPEC	SD_SPEC3	SD_SPEC4	SD_SPECX	SD PHYSICAL LAYER SPECIFICATION Version Number
0	0	0	0	Version 1.0 and 1.01
1	0	0	0	Version 1.10
2	0	0	0	Version 2.00
2	1	0	0	Version 3.0X
2	1	1	0	Version 4.XX
2	1	0 or 1	1	Version 5.XX
2	1	0 or 1	2	Version 6.XX
Others				Reserved

・DATA_STAT_AFTER_ERASE

This indicates the block “0” or “1” after erase operation.

・SD_SECURITY

Describe the security algorithm supported by the Card.

Table 23-3: Supported Security Algorithm

SD_SECURITY	Supported Security Specification
0	No Security
1	Not used
2	Version 1.01
3	Version 2.0
4	Version 3.xx
5-7	Reserved

・SD_BUS_WIDTHS

Indicates the DAT bus width that a supported by this card.

Table 23-4: Supported Bus Widths

SD_BUS_WIDTHS	Supported BUS width
0 bit position	1 bit(DAT0)
1st bit position	Reserved
2nd bit position	4 bit(DAT0-3)

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3rd bit position	Reserved

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・EX_SECURITY

This field indicates Extended Security which will be defined by a later version of the Part3 Security Specification Version 4.00.

Table 23-5: Extended Security

EX_SECURITY	Extended Security
0000b	Extended Security is not supported
Others	Extended Security is supported. The value of the field is specified by the Part3 Security Specification

・CMD_SUPPORT

Support bit of new commands are defined to Bit35-32 of SCR.

Table 23-6: CMD_SUPPORT

SCR_bit	Support Command	Command	CCC	Remarks
35	Extension Register Multi-Block	CMD58/59	11	Optional. If CMD58/59 is supported, CMD48/49 shall be supported.
34	Extension Register Single Block	CMD48/49	11	Optional
33	Set Block Count	CMD23	2,4	Mandatory for UHS104 Card
32	Speed Class Control	CMD20	2,4	Mandatory for SDXC Card

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7.4.4. SD Status

・DAT_BUS_WIDTH

Indicate the currently defined data bus width that was defined by SET_BUS_WIDTH command.

Table 24-1: DAT_BUS_WIDTH

DAT_BUS_WIDTH	Bus Width
'00'	1 bit(default)
'01'	Reserved
'10'	4 bit width
'11'	Reserved

・SECURED_MODE

Indicates whether card is in secure mode operation.

Table 24-2: SECURED_MODE

SECURED_MODE	Secured Mode Status
'0'	NOT Secured Mode
'1'	Secured Mode

・SD_CARD_TYPE

SD Card type described here.(Various SD types to be defined in the future.)

Table 24-3: SD_CARD_TYPE

SD_CARD_TYPE	SD Card Type
'0000'h	SD Memory Card

・SIZE_OF_PROTECTED_AREA

Show the size of protected area.

・SPEED_CLASS

This 8-bit field indicates the Speed Class.

Table 24-4: SPEED_CLASS

SPEED_CLASS	Speed Class
00h	Class 0
01h	Class 2
02h	Class 4
03h	Class 6
04h	Class 10
05h – FFh	Reserved

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・PERFORMANCE_MOVE

This 8-bit field indicates Performance of move and the value can be set by 1 [MB/s] step.

Table 24-5: PERFORMANCE_MOVE

PERFORMANCE_MOVE	Performance of Move
00h	Not Defined
01h	1 [MB/s]
02h	2 [MB/s]
.....	.....
FEh	254 [MB/s]
FFh	Infinity

・AU_SIZE

This 4-bit field indicates AU Size and the value can be selected in power of 2 from 16 KB.

Table 24-6: AU_SIZE

AU_SIZE	Size of AU
0h	Not Defined
1h	16 KB
2h	32 KB
3h	64 KB
4h	128 KB
5h	256 KB
6h	512 KB
7h	1 MB
8h	2 MB
9h	4 MB
Ah	8MB
Bh	12MB
Ch	16MB
Dh	24MB
Eh	32MB
Fh	64MB

The maximum AU size, depends on the card capacity, is defined in Table 24-7.

Table 24-7: Maximum AU_SIZE

Capacity	up to 64MB	up to 256 MB	up to 512 MB	up to 32 GB	up to 2TB
Maximum AU Size	512 KB	1 MB	2 MB	4 MB	64MB

Application Notes:
The host should use the maximum AU Size (4 MB) to determine host buffer size.
The host can treat multiple AUs combined as one unit.

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·ERASE_SIZE

This 16-bit field indicates N_{ERASE}. When N_{ERASE} numbers of AUs are erased, the timeout value is specified by ERASE_TIMEOUT. The host should determine proper number of AUs to be erased in one operation so that the host can indicate progress of erase operation.

Table 24-8: ERASE_SIZE

ERASE_SIZE	Erase Size
0000h	Erase Time-out Calculation is not supported.
0001h	1 AU
0002	2 AU
0003	3 AU
.....	.....
FFFFh	65535 AU

·ERASE_TIMEOUT

This 6-bit field indicates the T_{ERASE} and the value indicates erase timeout from offset when multiple AUs are erased as specified by ERASE_SIZE. The host can determine timeout for any number of AU erase by the Equation below.

Erase Time-out of X AU $= T_{ERASE}/N_{ERASE} \times X + T_{OFFSET}$

Table 24-9: ERASE_TIMEOUT

ERASE_TIMEOUT	Erase timeout
00	Erase Time-out Calculation is not supported.
01	1 [s]
02	2 [s]
03	3 [s]
….....	….....
63	63 [s]

·ERASE_OFFSET

This 2-bit field indicates the T_{OFFSET} and one of four values can be selected. The erase offset adjusts the line by moving in parallel on the upper side. This field is meaningless if ERASE_SIZE and ERASE_TIMEOUT are set to 0.

Table 24-10: ERASE_OFFSET

ERASE_OFFSET	Erase offset
0h	0 [s]
1h	1 [s]
2h	2 [s]
3h	3 [s]

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・UHS_SPEED_GRADE

This 4-bit filed indicates the UHS mode Speed Grade. Reserved values are for future speed grades larger than the highest defined value. Host shall treat reserved values (undefined) as highest grade defined.

Table 24-11: UHS_SPEED_GRADE Field

UHS_SPEED_GRADE	Value Definition
0h	Less than 10MB/s
1h	10MB/s and above
2h	Reserved
3h	30MB/s and above
4h-Fh	Reserved

・UHS_AU_SIZE

This 4-bit field indicates AU Size for UHS-I card and the value can be selected from 1MB.

Table 24-12: UHS_AU_SIZE Field

UHS_AU_SIZE	Value Definition
0h	Not defined
1h-6h	Not Used
7h	1M
8h	2M
9h	4M
Ah	8M
Bh	12M
Ch	16M
Dh	24MB
Eh	32MB
Fh	64MB

・VIDEO_SPEED_CLASS

This 8-bit field indicates the Video Speed Class supported by the card.

Table 24-13: VIDEO_SPEED_CLASS Field

VIDEO_SPEED_CLASS	Value Definition
0 (=00h)	Video Speed Class 0 (Video Speed Class is not supported)
6 (=06h)	Video Speed Class 6
10 (=0Ah)	Video Speed Class 10
30 (=1Eh)	Video Speed Class 30
60 (=3Ch)	Video Speed Class 60
90 (=5Ah)	Video Speed Class 90
Others	Reserved

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・VSC_AU_SIZE

This 10-bit field indicates the AU Size for Video Speed Class recording.
Please check the SD Physical Layer Specification for details.

Table 24-14: VSC_AU_SIZE Field

VSC_AU_SIZE	Value Definition
0	Video Speed Class is not supported
1 to 1023 (=3FFh)	AU Size for Video Speed Class of the card in unit of [MB]

・SUS_ADDR

This 22-bit field indicates a valid suspension address in 512KB units.

Table 24-15: SUS_ADDR Field

SUS_ADDR	Value Definition
0	No valid suspension address
Non-zero	valid suspension address in 512KB units

・APP_PERF_CLASS

This 4-bit field indicates the Application Performance Class supported by the card.

Table 24-16: APP_PERF_CLASS Field

APP_PERF_CLASS	Value Definition
0	Application Performance Class is not supported
1h	A1, Application Performance Class level 1
2h	A2, Application Performance Class level 2
3h - Fh	Reserved

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・PERFORMANCE_ENHANCE

This 8-bit field indicates the performance enhancement functionalities supported by the card.

Table 24-17: PERFORMANCE_ENHANCE Field

APP_PERF_CLASS	Value Definition
SD_STATUS b[335:331]	0h:Command Queue is not supported 1h:Command Queue supported, with queue depth 2 2h: Command Queue supported, with queue depth 3 ….. 1Fh: Command Queue supported, with queue depth 32
SD_STATUS b[330]	Support for Cache 0: Not Supported 1: Supported
SD_STATUS b[329]	Support for Host-initiated maintenance 0: Not Supported 1: Supported
SD_STATUS b[328]	Support for Card-initiated maintenance 0: Not Supported 1: Supported

・DISCARD_SUPPORT

This 1-bit field indicates the DISCARD operation supported by the card.

Table 24-18: DISCARD_SUPPORT Field

DISCARD_SUPPORT	Value Definition
0	Not Supported
1	Supported

・FULE_SUPPORT

This 1-bit field indicates the FULE operation supported by the card.

Table 24-19: FULE_SUPPORT Field

FULE_SUPPORT	Value Definition
0	Not Supported
1	Supported

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8. Others: Limited Conditions, SD Specification Compliance

1) Non Supported Registers:
DSR Register (Optional register: PHYSICAL LAYER SPECIFICATION Ver.6.10)

2) Non Supported Functions:
Programmable Card Output Driver (Optional in PHYSICAL LAYER SPECIFICATION Ver.6.10)
Card's Internal Write Protect (Optional in PHYSICAL LAYER SPECIFICATION Ver.6.10)

3) Non Specified Command:
CMD4 SET_DSR
CMD56 GEN_CMD

4) Optional Security Feature
This card will not support any security command except for ACMD44. For all security commands mentioned below, the card shall either set ILLEGAL_COMMAND error bit or ERROR bit in the status register.
ACMD18, ACMD25, ACMD26, ACMD38, ACMD43, ACMD45, ACMD46, ACMD47, ACMD48.

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9. Host System Design Guidelines

The purpose of this guideline is a reference to help the design of the SD Memory Card interface of the Host system.

The description here does not make any warranty fitness for particular host.
The implementations of the host systems are different in each system.
Please design the SD Memory Card Host systems considering the each condition.

Mandate: Mandate requirement to the Host implementation
Recommendation: Recommended Implementation, Just General Example

9.1. Retry after Memory write (Mandate)

Please issue the ACMD22 and check written blocks if it occurs error by checking the written blocks after Memory write. (CMD25: WRITE_MULTIPLE_BLOCK)
Please retry CMD25 blocks if written blocks are different from your expectation.

Background

The Flash Memory used in this card has possibility of Memory Write (Program) Error.
If the Memory Write Error occurs in some memory page, the Write error may impacts other pages in the same block.

9.2. SPI-Mode initialization (Mandate)

SD Card shall be initialized by ACMD41. Do NOT use CMD1 for SPI-Mode initialization.

9.3. SPI-Mode RSV pin Pull up (Mandate)

RSV (#1, #8 in SPI Mode) shall be pulled up by 10-100k-ohm resistors.
(See **6.1. microSD Card Pins**)

9.4. Prohibition during Write (Mandate)

Do not turn off the power or remove the SD Memory Card from the slot before read / write / erase / mutual authentication operation is complete. Avoid using the SD Memory Card when the battery is low. Power shortage, power failure and/or removal of the SD Memory Card from the slot before read/write/mutual authentication operation is complete will cause malfunction of the SD Memory Card, loss of data and/or damage to data.

Please comment and inform this prohibition to the end users in proper way. (Manual or Instructions)

9.5. Process after Timeout in case of Read or Write (Recommendation)

If there are no-response after the timeout passed in case of read or write (Recommendation), please issue the CMD12(Stop Transmission) and stop the data transfer to prevent the host stuck on waiting for the response.

(Reference: 7.3.3. Data Token, 7.3.4.Data Error Token of SD PHYSICAL LAYER SPECIFICATION.)

In case of SPI mode, there are some restrictions regarding to access the out of range boundary.

1) Response error (*1) will be occurred when host issue CMD12 over the out of range boundary under WRITE_MULTIPLE (CMD25, ACMD25) action.
   Host should neglect CMD12 error status.

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2) This maybe occurred when SD CLK is low frequency.
In case of out of range token maybe duplicated, please check case (a) and case (b) when issue CMD12 after reading before the boundary using READ_MULTIPLE (CMD18, ACMD18).

(a) Response error maybe occurred (*1)
(b) Response of CMD12 maybe not issued.

- Re-issue CMD12, then next command can be received
- Neglect the response of re-issue CMD12

*1: Response Error Descriptions

- If CRC Check is On.

  Com CRC Error is responded.

- If CRC Check is Off.

  In case of 1) above, R1=0x44(Parameter Error & Illegal Command).
  In case of 2) above, R1=0x44(Illegal Command).

9.6. SD Command (Mandate)

1) CMD0 continuously issue
Do NOT continue the CMD0 with 1Pin (CD/DAT3) ='Low' just after CMD0
or the SD Card initialized in SPI mode.
In case of 1 pin (CD/DAT3) ="Low", it means SPI mode so be careful to the duration of CMD0 issue.
Please choose the appropriate timing interval for CMD0 to prevent this problem.
The interval is related with the pull up Resister value. Of the host side.

2) After the Security Read Command
Please issue the CMD13 to ensure the status change to the transmission state
or wait more than 100 μs, after issue the ACMD18 or ACMD43.

3) CMD12 (SD mode) or 'Stop Tran Token' (SPI mode) after Multiple Block Write Command
When the CMD12 (STOP_TRANSMISSION, SD mode) or 'Stop Tran Token' (SPI mode) is issued after Multiple Block Write Command (CMD25, ACMD25), please issue the CMD12 or 'Stop Tran Token' immediately (*) after the last data block, to complete the data write transaction soon.
(*)It should be within 400 μs after the end of BUSY status for the last data block.

4) Time Interval between successive SD commands
Time interval between the BUSY end of the SD command and the start bit of the next SD command should be more than 15 μs.
If the time interval is less than 15 μs, SD bus error or device operation error may occur occasionally.

9.7. Pull Up resistors (Recommendation)

CMD and DAT [3:0] can pull up with 10-100k ohm resistors by the host side.
Pleased disable the Card-Internal pull up on CD by ACMD42 before access. (Refer Fig. 7)

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10. Reliability Guidance

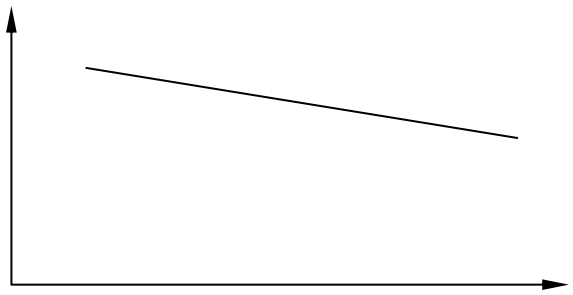
This reliability guidance is intended to notify some guidance related to using raw NAND flash. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

-Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

-Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Also write/erase endurance deteriorates data retention capability. The figure below shows a generic trend of relationship between write/erase endurance and data retention.



-Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Considering the above failure modes, KIOXIA recommends following usage:

- Please avoid any excessive iteration of resets and initialization sequences (card identification mode) as far as possible after power-on, which may result in read disturb failure. The resets include hardware resets and software resets.

e.g.1) Iteration of the following command sequence, CMD0 - ACMD41 --- The assertion of ACMD41 implies a count of internal read operation in Raw NAND.

CMD0: Go idle state command, ACMD41: SD send operation command

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Appendix 1: microSD Card Mechanical Dimensions (Unit : mm)

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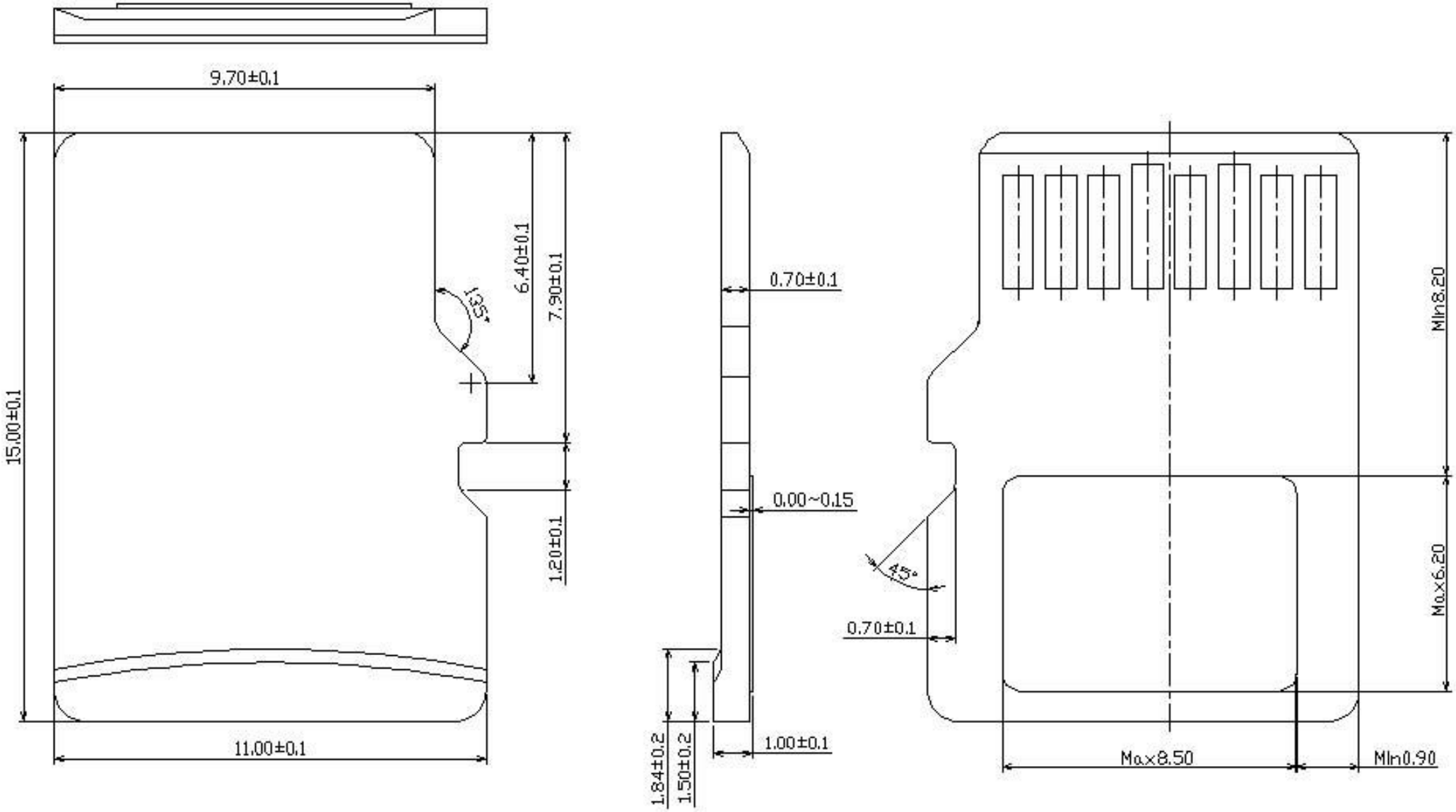

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Appendix 2: Memory Map and Dump Data of User Data Area

Last address of this memory map indicates “actual last address + 1”.

0x000000000(4096KB)	Master Boot Record and Partition table
	0000000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00) 00001b0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 82 00001c0 03 00 0c fe ff ff 00 20 00 00 00 60 cf 01 00 00 00001d0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00) 00001f0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa 0000200 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00)
0x000400000(0.5KB)	Partition Boot Sector
	0400000 eb 00 90 xx xx xx xx xx xx xx xx 00 02 40 0a 03 0400010 02 00 00 00 00 f8 00 00 3f 00 ff 00 00 20 00 00 0400020 00 60 cf 01 7b 0e 00 00 00 00 00 00 02 00 00 00 0400030 01 00 06 00 00 00 00 00 00 00 00 00 00 00 00 00 0400040 80 00 29 xx xx xx xx 4e 4f 20 4e 41 4d 45 20 20 0400050 20 20 46 41 54 33 32 20 20 20 00 00 00 00 00 00 * (All 0x00) 04001F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa
0x000400200(0.5KB)	FS Info Sector
	0400200 52 52 61 41 00 00 00 00 00 00 00 00 00 00 00 00 0400210 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00) 04003e0 00 00 00 00 72 72 41 61 ff ff ff ff 02 00 00 00 04003F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa
0x000400400(0.5KB)	Reserved for boot sector
	0400400 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00) 04005F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa
0x000400600(387.5KB)	
	0400600 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00) 0400C00-0400DFF : Partition Boot Sector(Backup) 0400E00-0400FFF : FS Info Sector(Backup) 0401000-04010FF : Reserved for boot sector(Backup) 0401200 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00)
0x000461400(1853.5KB)	FAT1
	0461400 f8 ff ff 0f ff ff ff 0f ff ff ff 0f 00 00 00 00 0461410 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00)
0x000630A00(1853.5KB)	FAT2
	0630A00 f8 ff ff 0f ff ff ff 0f ff ff ff 0f 00 00 00 00 0630A10 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00)
0x000800000(15,179,776.0KB)	UserData
	0800000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 * (All 0x00)
0x39F000000	Last Address(+1)

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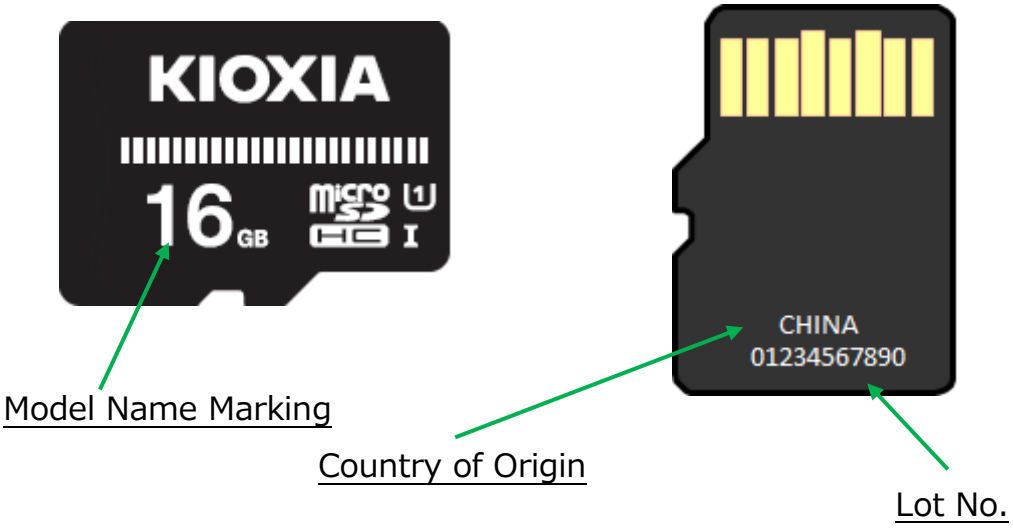
Appendix 3: Marking



“Model name marking”:

CAPACITY	MODEL NAME	MARKING
16GB	SD-C16G3K1A(AHHYA)	16GB

“Lot No.”: 11 letters

4 “weekly codes” + 6 “serial No.” + 1 “Card Version”

“Origin country”: CHINA

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Appendix 4: For Instruction Manual

Please comment and inform this prohibition to the end users in proper way. (Manual or Instructions).

Notes on usage

- The Card contains nonvolatile semiconductor memory. Do not use the Product in accordance with a method of usage other than that written in the manual. This may cause the destruction or loss of data.
- To protect against accidental data loss, you should back up your data frequently on more than one type of storage media.
  **** Corporation assumes no liability for destruction or loss of data recorded on the Card for any reason.
- Please use the Product only with general home and office equipment such as digital cameras, PDAs, printers, personal computers, mobile phones and similar devices. KIOXIA assumes no liability for damage or losses due to use of the Product with equipment other than these kinds of general home and office devices/equipment. The Product shall not be used with equipment (including but not limited to atomic energy control, airplane or spaceship, transportation, traffic signal, combustion control, or medical instruments, as well as all types of safety devices) that requires extraordinarily high quality and/or reliability, or equipment a malfunction or failure of which may cause loss of human life or bodily injury.
- When used over a long period of time or repeatedly, the reading, writing and deleting capabilities of the Product will eventually fail, and the performance speed of the Product may decrease below the original speed specific to the Product's applicable class.
- With limited exceptions, including use for one’s personal enjoyment, recorded music cannot be used without permission from the holder of the appropriate rights. Please refer to copyright laws appropriate to your country or region.
- If the Card is to be transferred or destroyed, note that the data it contained may still be recoverable unless it is permanently deleted by third-party deletion software or similar means beforehand. Please comply with local government regulations when disposing of the Product.
- Do not attach labels to the Card or Adapter as this could hinder or prevent insertion or removal of the Product.
- When inserting the Card into the Adapter, first confirm that the Card is correctly oriented for insertion, as shown in the figure to the right, in order to avoid damaging the Card or the Adapter.

Limitation of Liability

- **** Corporation assumes no liability for damage or losses due to fire, earthquake, natural disaster, accident, acts of third parties, or negligent or intentional misuse.
- **** Corporation assumes no liability for damage or losses, lost profits, or third party claims arising out of the use of, or inability to use, the Product.
- **** Corporation assumes no liability for damage or losses occurring as a result of noncompliance with the instructions in the enclosed product manual.
- **** Corporation assumes no liability for destruction or loss of data occurring during use of the Product, regardless of the cause, type, or scale of damage.
  Note: **** Corporation will not perform restoration or recovery of data.
- **** Corporation assumes no liability for damage or losses occurring due to malfunctions resulting from a combination of connected devices and software

Cautions

- Do not bend, crush, drop, or place heavy objects on top of the Product. Do not use tweezers, pliers, or similar items that could damage the Product. Take particular care when inserting or removing the Product. Stop using the Product when the Product does not work properly. Failure to follow these instructions could result in fire, damage to the Product and/or other property, and/or personal injury including burns and electric shock.
- Keep out of reach of small children.

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Accidental swallowing may cause suffocation or injury.
Contact a doctor immediately if you suspect a child has swallowed the Product.

- If the Product produces noises, an odor, overheats or smokes, turn off the computer and peripherals immediately and disconnect the power cord/cable from the power plug socket, and do not touch the Product. Failure to follow these instructions could result in fire, damage to the Product and/or other property, and/or personal injury including burns and electric shock. Do not use the Product again. Please contact the store that you purchased the Product from.

Exercise caution when handling the Product.

- Do not directly touch the interface pins, put them in contact with metal, strike them with hard objects, or cause them to short. Do not expose to static electricity.
- Do not disassemble or modify the Product. This may cause electric shock, damage to the Product, or fire.
- Do not expose the Product to moisture. Do not use or store the Product in locations where conditions exceed operating condition stipulations for temperature or humidity. Do not place the Product in a dusty location, in a location where there is static electricity, electrical noise, or strong magnetic fields, in a location exposed to corrosive chemicals or gases, or near sources of heat or flame. Do not heat the Product or place it in a fire. Do not allow the interface pins to become dirty.
- While writing data to or reading data from the Card, do not shake or cause an impact, turn off the power, remove the Card from the Adapter, remove the Adapter from the device, or permit the Product or device to be shaken or impacted.
- Do not insert or remove the Card while the Adapter is still inserted into a device.
- Do not insert into a device the Adapter that does not contain the Card.
- Do not insert anything other than the Card into the Adapter.

Instructions

- The Card comes pre-formatted in compliance with SD Memory Card standards. Reformatting the Card will cause all data stored in the Card to be lost. Before reformatting, please back up all data you wish to save. Formatting with a personal computer or a device not compliant with SD Memory Card standards may cause problems with the Product such as the inability to read, write, or delete data.
- Refer to your device's manual to learn how to use the Products.
- Insert the Product firmly in the correct orientation. The Product will not operate correctly if it is inserted in an incorrect orientation or not inserted all the way.
- Always use the Adapter when using the Card with a standard SD memory card device. Inserting the Card directly into a standard SD memory card device may cause the Card or device to malfunction.

microSDHC Logo is a trademark.

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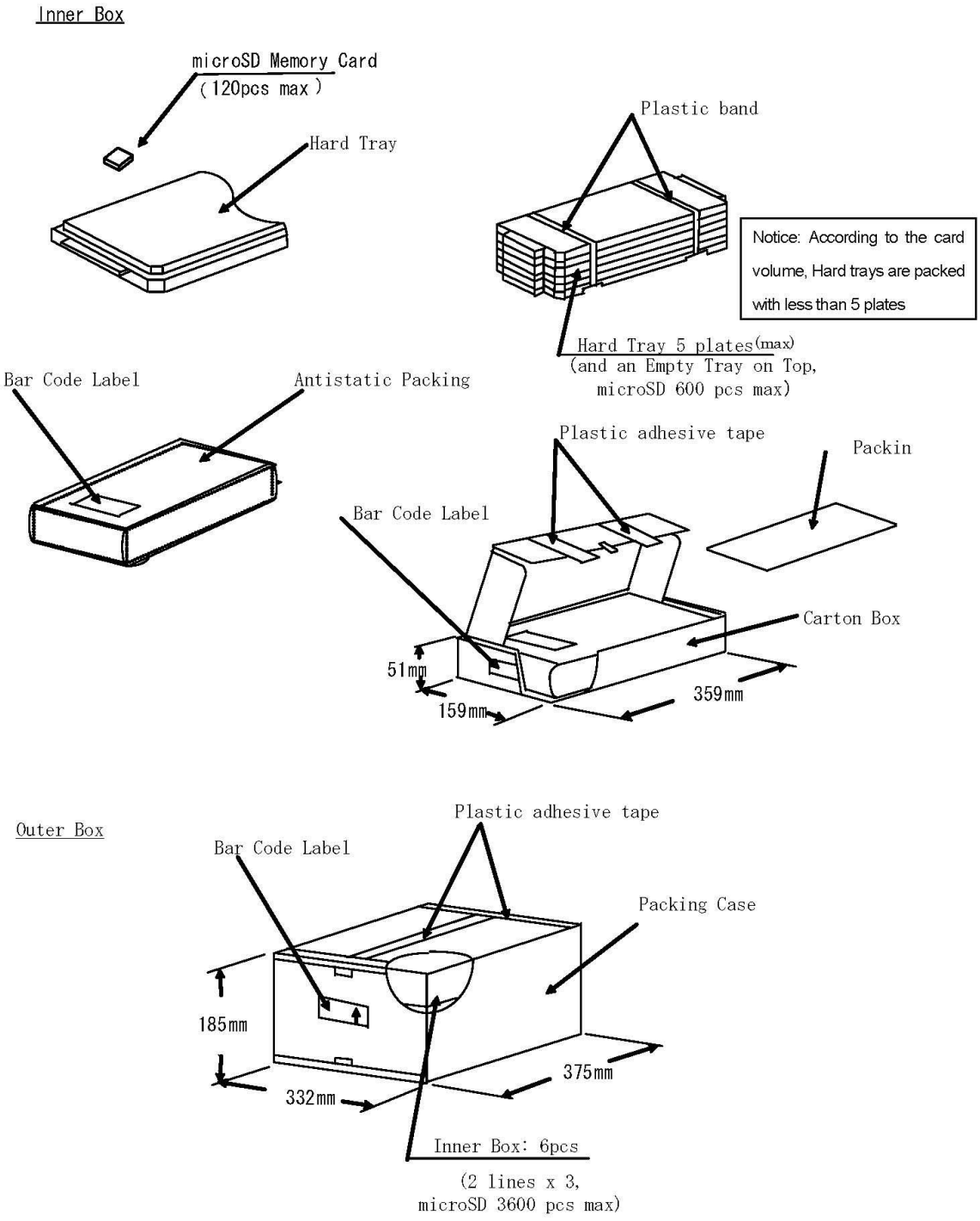
Appendix 5-1: Shipping Package



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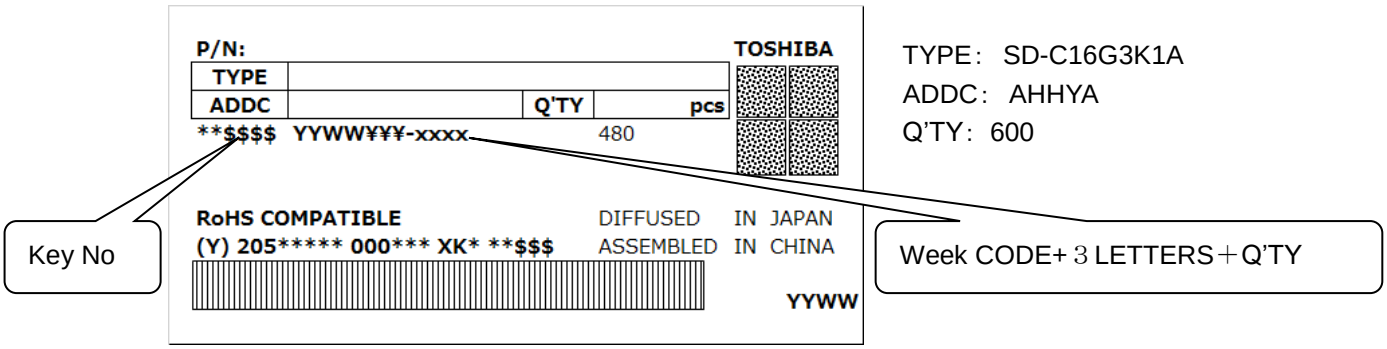
Appendix 5-2: LABEL DETAIL（600pcs BOX, 3600pcs BOX）



1) Model Name

Model Name	TYPE	ADD.C	Capacity
SD-C16G3K1A (AHHYA)	SD-C16G3K1A	AHHYA	16GB

2) LOT
For the control of production or shipment
Different by production and shipment

3) Quantity

* Inner Box
Max 600pcs
（including dummy tray according to circumstances）

* Outer Box
Max 3,600pcs
（including empty box or buffer materials according to circumstances）

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Appendix 6: FACTORY, PRODUCING COUNTRY

・Country of origin : Diffused in JAPAN
Assembled in CHINA

・Producing works
Pellet process : KIOXIA Corporation
YOKKAICHI Operation
／800, YAMANOISSHIKI-CHO, YOKKAICHI, MIE-PREF, 512-8550
Assembly process : Amkor Technology
／Bldg No.2, 52 Fasai Road, Waigaoqiao Free Trade Zone.
Pudong, Shanghai, 200131 PRC

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